POWER ON RESET TECHNIQUES FOR AN INTEGRATED CIRCUIT CHIP

Abstract of the Disclosure

A power on reset circuit, preferably for an integrated circuit, detects application of voltage, starts a phase locked loop one application of voltage is detected but inhibits all clock used for digital logic operations until voltage stability is achieved. If a switched converter is used, the duty cycle of the switched converter is held at unity for a period of time before it is set to that needed to achieve the desired chip operating voltage. Clocks controlling other circuits can be released in stages after the duty cycle of the switched converter is set to its operating voltage level.